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Design and Analysis of CMOS-Memristor-Based Inverter Circuits for Low-Power and High-Efficiency Logic Applications

Arul C[1] and Dr. Omkumar S[2]
[1]Research Scholar, Department of Electronics and Communication Engineering, SCSVMV University, Kanchipuram, India.
Email: arulbpt12@gmail.com
[2]Associate Professor, Department of Electronics and Communication Engineering, SCSVMV University, Kanchipuram, India.
Email: omkumar1234@gmail.com

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Abstract
Deep learning techniques can be utilized to process high-definition video of real-world events through two distinct approaches. One such approach involves the use of Spiking Neural Networks (SNNs), a specialized type of neural network. SNNs are particularly advantageous due to their low power consumption and ability to perform simple mathematical computations using spike-based signals. However, the asynchronous nature of spike alignment may present challenges in training when implemented with hardware components. Alternatively, Complementary Metal-Oxide-Semiconductor (CMOS) neural networks can be trained using the conventional backpropagation algorithm. Nevertheless, this method may incur significant additional costs due to the need for specialized hardware and increased power consumption. Moreover, substantial memory resources, such as Static Random-Access Memory (SRAM), are required to maintain temporal data over extended periods. Recent advancements have demonstrated that memristors, when integrated with CMOS technology, can facilitate the development of event-driven neural networks within electronic systems. This hybrid architecture employs both spike-based processing and traditional backpropagation methods. Key components of such neural networks include synaptic crossbars, input neurons, hidden neurons, and output neurons, all of which are implemented using mixed-signal circuits. Initially, the newly configured neural cells are prepared to process input from Dynamic Vision Sensor (DVS) cameras. Input/output (I/O) neurons, composed of memristors, convert event-based data into columnar formats using simple locking mechanisms. The artificial neural network (ANN) comprises memristor crossbars that emulate synaptic behavior, facilitating data processing as the input graph evolves. This approach ensures efficient event filtering and data refinement. Owing to the intrinsic relationship between current and voltage in memristors, the crossbars can perform multiply-accumulate (MAC) operations with minimal power consumption. Furthermore, hidden and output neurons are capable of transforming the columnar currents within the crossbars into output voltages when the Rectified Linear Unit (ReLU) activation function is applied. In scenarios with high event-processing demands, the frequency of MAC operations can be dynamically adjusted. To enhance power efficiency, the

system is designed to autonomously disable the MAC calculation clock when not in use. Experimental validation using the MNIST-DVS and POKER-DVS datasets indicates that the proposed neural network architecture achieves a reduction in power consumption by approximately 0.5%, although it exhibits slightly reduced performance on the POKER-DVS dataset. Compared to traditional methods, the new approach demonstrates a 0.75% decrease in accuracy on the MNIST-DVS dataset. Nevertheless, the proposed design offers up to 75% power savings, albeit with a minor compromise in performance.

Keywords: Challenges in Memristor Integration, Applications of Memristors, Memristor for Applications in Neuromorphic and Edge Computing.

1. Introduction

Memristors, an abbreviation for "memory resistors," possess the unique ability to retain information about the amount of electrical power that has previously passed through them. The concept of memristors was first introduced by Leon Chua in 1971. According to Chua, memristors represent the fourth fundamental passive circuit element, following resistors, capacitors, and inductors. Unlike these traditional components, memristors exhibit a property known as memristance, allowing their resistance to vary based on the history of electrical energy applied to them. This distinctive characteristic makes memristors particularly suitable for applications in neural networks, non-volatile memory systems [1], and other memory technologies where historical data retention is advantageous. Memristors can emulate the natural connectivity patterns of brain cells, reflecting how electrical signals have previously traversed neural pathways. Consequently, they hold potential for the development of neuromorphic computing systems, which are designed to mimic the architecture and functioning of the human brain.

In 2008, researchers at Hewlett-Packard (HP) Laboratories advanced the concept of the memristor by demonstrating a functional prototype. Their design featured a layered structure comprising titanium dioxide (TiO_2) and oxygen-deficient titanium dioxide (TiO_2-x), positioned between two platinum electrodes. This prototype functioned in alignment with the theoretical model proposed by Leon Chua, establishing a direct relationship between magnetic flux (Φ) and electric charge (q) [2]. The memristor operates by transitioning between two distinct resistance states: High Resistance State (HRS) and Low Resistance State (LRS). These states can be modulated by applying varying levels of electrical power. The LRS corresponds to the resistance state denoted as RONRON, while the HRS aligns with the $ROFF$R OFF resistance state. When the memristor is set to the LRS, it permits a significant flow of current, representing a logical '1'. Conversely, in the HRS, the current flow is minimal, corresponding to a logical '0'. This variability in resistance enables the memristor to store and retain information. A key characteristic of memristors is their non-volatile nature. When power is removed, the memristor maintains its resistance state. Upon restoration of power, the device quickly reverts to its previous resistance value, as it inherently retains the last recorded resistance level. This unique ability to preserve resistance values makes memristors particularly advantageous for data storage applications and other advanced electronic devices [3].

Williams and Chua assert that memory devices and sensitive devices are fundamentally the same. This classification is independent of their operational mechanisms or material composition. It is important to explore technologies that are resistant to electrical damage, as outlined in the provided list. Understanding how to protect these devices is crucial and can

facilitate more effective categorization. These devices may include ferrous materials, phase-change materials, and even biological components. Some researchers have also suggested that memory plays a critical role in these systems, regardless of their function or mode of operation [4]. Complementary Metal-Oxide-Semiconductor (CMOS) technology has been the most prominent since the advent of integrated circuits three decades ago. CMOS is highly regarded for its rapid performance, low power consumption, and the ability to integrate numerous components into a single unit. As CMOS Very-Large-Scale Integration (VLSI) technology advances, transistor sizes continue to decrease. However, merely scaling up the number of components is not a sustainable solution in the long term. The manufacturing process of CMOS chips presents several inherent flaws and limitations, such as constraints in spatial capacity and technical capabilities for printing and other fabrication processes. These challenges and limitations could pose significant obstacles to further development.

Moore's Law and the strategies for technological advancement must continue to evolve and improve. As nanoscale devices [5] were developed, there was a prevailing belief that CMOS technology could be further optimized. This is one of the key reasons why memory-based technologies present distinct advantages and potential applications. The memristor, for instance, functions effectively despite its compact size of only 10 nm. Its reduced dimensions and increased operational speed are made possible by the complementary interaction between CMOS technology and memristors [22]. This innovative and unique component holds potential for integration into custom-designed power systems. Currently, the demand for compact, energy-efficient devices is growing significantly, and these technologies could offer viable solutions. Memristive circuits have diverse applications, including memory storage, neuromorphic computing systems, logic gates, and analog circuits [6]. A particularly noteworthy characteristic of the memristor is its non-volatile nature, which is fundamental in the development of Resistive Random Access Memory (RRAM) [7]. To advance information and communication technologies (ICT), it is essential to adopt new methodologies and tools for the design of digital logic units. The appeal of simple logic gates with memory capabilities has contributed to the increasing interest in this area. In recent years, researchers have explored the use of memristors to enhance logic circuit functionality.

The project, titled "Memory Logic," aims to integrate memristors into logic gates, enabling them to function similarly to traditional components. When the FALSE gate is combined with IMP logic [23], it becomes possible to implement all universal logic gates. Alternatively, memristors can be utilized as the sole logic gates. This configuration of nanowires is referred to as an "x-bar setting," wherein a memristor [8] can switch between two nanowires. This concept forms one of the foundational principles of the proposed approach. In the memristor-based logic families discussed, logic values are stored as resistance. However, this is not universally applicable. In some cases, only the value can be stored, and memristors serve as the exclusive components for performing computations. Prior to this work, CMOS and memristor circuitry had never been integrated. The successful operation of this system relies exclusively on CMOS and memristors [9]. A significant limitation arises from the fact that the gates cannot retain the last transmitted value, leading to system failures. Furthermore, this approach is inadequate because NAND and NOR gates cannot be constructed without the conventional CMOS inverter gate.

This paper presents a hybrid CMOS and memristor-based inverter gate, representing an

advancement over previous logic gates that were limited to arithmetic operations. The design integrates CMOS technology with memristors to achieve enhanced functionality. Unlike traditional gates, this inverter gate incorporates the ability to determine subsequent operational pathways. A key metric of interest is the amount of unused energy, as it directly relates to the gate's efficiency. This inverter gate serves as a fundamental component in the development of basic logic gates, which can subsequently be configured to perform AND or OR operations. This can be achieved through the implementation of alternative CMOS inverter gate designs.

Static Random Access Memory (SRAM) is a critical component in numerous technological applications. One of the primary considerations in the design of such devices is their intended application [10]. With the increasing use of SRAM in compact projects, there is a growing interest in understanding the power consumption requirements of SRAM cells. The efficiency of the proposed method is influenced by the size of the SRAM, with varying performance outcomes. Most computer systems allocate significant space for SRAM platforms, and power dissipation is closely linked to the dimensions of the SRAM chips utilized in larger systems. Additionally, the total number of SRAM cells plays a crucial role in determining overall power consumption.

The 6T SRAM cell is widely utilized in various applications. However, due to the nature of data retention in these cells, information is lost when power is interrupted. Additionally, the 6T SRAM cell consumes more power, as it requires a longer startup time [11]. To enhance the performance and reliability of SRAM cells, many researchers have incorporated non-volatile memory technologies, which retain data even during power outages. The power consumption, durability, and response time of SRAM cells are influenced by factors such as cell geometry, the number of cells, and their interconnections [24]. Reducing power consumption may adversely affect the cell’s lifespan. When operating in sub-threshold mode, circuits function below the threshold voltage, which can lead to reduced stability and increased sensitivity to power fluctuations, particularly in smaller devices [12]. This mode of operation may also limit the availability of power sources. As device dimensions continue to shrink, certain modifications do not necessarily yield performance improvements. Variations in Oxide Thickness (OTV) and Line Edge Roughness (LER) can contribute to these challenges, complicating the stability of SRAM cells. To address these limitations, memristors were introduced. Memristive components, characterized by their non-volatile nature, are capable of retaining their programmed state even after power has been removed.

2 Related work

Advancements in CMOS technology have led to increased circuit complexity, resulting in issues such as leakage currents, reduced circuit stability, and higher power consumption. Consequently, the primary focus is no longer solely on achieving high-speed performance with minimal power usage. Currently, efforts are directed towards enhancing computational speed while ensuring devices remain compact, efficient, and power-conscious. One promising approach involves in-memory computing as an alternative to the traditional Von Neumann architecture, which is increasingly seen as a limiting factor. In recent years, memristors have been utilized in various applications, including chaotic circuits [13], neural networks, and digital circuits. Memristors have been associated with multiple computational paradigms, such as Memristor Ratioed Logic (MRL) and Memristor-Aided Logic (MAGIC). However, MAGIC

logic faces inherent limitations in scalability, ceasing to function effectively beyond a certain point. This phenomenon occurs because the resistance of memristors is determined by the partial voltage across series resistors. Exceeding the optimal voltage threshold risks data corruption during processing. Furthermore, IMPLY logic, another memristor-based computing method, requires additional operational steps, which restricts its overall computational capabilities.

The design allows for switching between functional and non-functional components, analogous to the operation of diodes and circuits. In this project, CMOS and memristor-based smart gates are employed to develop the next generation of circuits [25]. Flip-flop technology has undergone significant advancements over time, enabling it to serve as an alternative to CMOS technology, which faces limitations related to chip size and power consumption. A compact flip-flop, designed by experts, can be activated using an implicit dual-edge pulse. To optimize clock management, the Modified Particle Swarm Optimization (MPSO) method was implemented, resulting in reduced latency for this flip-flop. Furthermore, the power requirements of the MOSFETs were minimized [14]. The use of a flip-flop with an enhanced pulse display contributes to transistor savings, leading to improved chip speed and reduced power consumption. This flip-flop, equipped with a display pulse, differs from existing models and is fabricated using a specific type of full-oxide thin-film circuit. Nanotechnology was applied to further reduce the chip's dimensions. Additionally, a carbon nanotube field-effect transistor can be utilized in place of a conventional CMOS transistor to construct a dynamic double-edge-triggered D flip-flop (DFF), resulting in lower power dissipation and faster response times.

Moore's Law [15] posits that as technology scales down in size, it simultaneously increases in performance and capacity. However, with the current CMOS technology, it is becoming increasingly challenging to adhere to this principle. While CMOS technology is efficient in terms of space and power consumption, limitations persist. The integration of CMOS with memristors has been proposed to enable the development of a linear feedback shift register, which would operate at high speeds while maintaining low power consumption. This design incorporates a greater number of transistors compared to previous models. At the nanometer and sub-nanometer scales, advancements have been made in the fabrication of integrated circuits (ICs), resulting in improved performance. Nevertheless, further research and development are necessary to enhance circuit interoperability and efficiency. Ensuring system functionality without thorough validation remains a challenge, often leading to increased costs and extended development timelines [15]. Integrated circuits can be verified and tested using Automatic Test Equipment (ATE). As an alternative, on-chip testing methodologies, such as built-in self-test (BIST), have been introduced. Additionally, the concept of hybrid logic built-in self-test (LBIST) has been explored. LBIST offers improved testing speeds compared to traditional methods, thereby presenting a more efficient solution for circuit validation.

The memristor is considered the fourth fundamental component of a circuit, linking magnetic flux and electric charge. This concept was first introduced in 1971 by Professor Leon Chua. In 2008, researchers at HP Labs significantly altered the operational understanding of the memristor. Since then, extensive research has been conducted to explore the capabilities

and applications of memristors. An HP memristor is composed of nanoscale titanium dioxide (TiO_2) structures. The device features both a doped region and an undoped region at its core. The dynamic resistance of this two-terminal component can vary within a specific range, shifting from low resistance (R) to high resistance (R). The resistance of the memristor is determined by the magnitude, direction, and duration of the charge applied across its terminals. Notably, the memristor retains its resistance state even after power is removed. Memristors can be manufactured using processes similar to those employed in the production of CMOS and MEMS technologies. Furthermore, MEMS devices consume no power when inactive, a characteristic shared by non-volatile memory (NVM) memristors, which enhances their efficiency. Due to their reconfigurability, memristors are valuable not only for energy storage and processing but also in a variety of machine-based applications.

The increasing demand for compact devices has driven the development of small, low-power components that can be integrated into integrated circuits (ICs) [16]. Technological advancements have enabled the miniaturization and enhancement of devices that were previously larger and less efficient. These improvements have significantly benefited personal computers and other compact electronic devices. However, the benefits predicted by Moore's Law are becoming less pronounced as more efficient tools emerge. In recent years, there has been growing interest in low-power edge computing. These devices allow data processing to occur locally, eliminating the need to transmit data to the cloud. This enables real-time analysis at the point of data collection, enhancing performance and efficiency. Additionally, devices with greater storage capabilities are becoming increasingly attractive, and the demand for enhanced computational power continues to rise. Despite these advancements, further research is required in this field, as edge computing remains a critical and evolving area of study.

2.1. Challenges in Memristor Integration

Memristors and their application in real-time systems remain emerging areas of study. Currently, many commercial products do not incorporate memristors. Furthermore, it is not advisable to purchase memristors at this stage due to the complexity involved in their development. Ensuring the stability of their long-term operational characteristics poses significant challenges. In contrast, memory cells are composed of various components that can function together in multiple configurations. This variability can lead to inconsistent performance [17]. Consequently, retailers face difficulties in marketing memristors, and their integration into widely recognized computing systems has been slow. Additionally, the composition and operational principles of memristors are not always transparent. The absence of standardized regulations complicates the development of uniform testing procedures and methodologies. As a result, assessing the interoperability of memristors produced by different manufacturers and research groups is challenging. These issues are still under investigation. To enhance their practical application, it is essential to standardize their fabrication processes. Consistent production methods will facilitate the evaluation of new concepts. By creating precise replicas and models of memristors, it may become possible to predict and analyze their behavior more accurately.

The development of improved tools for memristors can benefit from CMOS technology. CMOS components can replicate the behavior of memristors due to the inclusion of CMOS transistors within their structure. However, authentic memristor designs offer several

advantages over these CMOS-based imitations. Modern CMOS fabrication techniques enable the creation of these memristor-like components, which consume less power and can be scaled to larger sizes, allowing for higher production volumes [18].

Unlike genuine memristor systems, which are costly and difficult to replicate, these CMOS-based alternatives offer a more accessible and efficient solution. It is important to consider these factors when discussing and working with memristor technologies. Nevertheless, CMOS-based memristors may demonstrate superior performance in certain applications. Additionally, tools and devices that incorporate memristors can be further optimized using CMOS technology. The memristor chip in question is fabricated using CMOS processes. It features a current-steering integrator (CSI) circuit capable of emulating the dynamic resistance behavior of a memristor. Furthermore, a memristor port may be integrated with various units to expand functionality. This type of circuit, also referred to as a floating-gate transistor (FGT) circuit, can be employed in high-speed applications.

2.2. Applications of Memristors

Memristors are not yet commercially available due to unresolved scientific challenges and the high costs associated with their development. One proposed approach involves modeling memristors in SPICE simulations. Additionally, alternative applications of CMOS technology in conjunction with memristors are being explored. The relationship between CMOS chips and SPICE models is integral to this research, as CMOS-based memristors cannot function without these components [19]. Some researchers suggest that memristors have the potential to repair or enhance CMOS units. Furthermore, there are two identified types of write circuits and three types of read circuits associated with memristor technology. Studies on memristor resistance indicate that its resistance is variable, and circuits designed to measure current are effective in this context. This functionality is attributed to the memristor's ability to switch between different states, as depicted in graphical representations of its resistance levels. Memristors possess the capability to retain information about their previous states, making them valuable for storing critical data without the risk of loss. Compared to traditional memory systems, MEMS (Micro-Electro-Mechanical Systems) memory offers advantages such as the ability to store non-binary code and reduced noise interference. The mechanisms through which memristors can retain new information remain an area of active interest, although these components are no longer utilized for their original purposes.

These components are integrated, allowing for efficient tracking of image data, which accelerates information processing. The value displayed on the screen [27] indicates a decreasing trend. Additionally, these components have been utilized in logic circuits, up-down counters with reduced transistor requirements, and full subtractors. Various sensors have been developed, including the Wien Bridge Oscillator, nanoscale memristor-based 2:1 multiplexer, neuro-memristive circuits for edge computing, and low-power wireless sensors designed for medical applications. These technologies facilitate connectivity within the Internet of Things (IoT). Unmanned Aerial Vehicles (UAVs) differ in that their wings provide the necessary lift for flight. Edge computing relies on the ability to acquire, process, and store data locally at the network's edge. "Edge-intelligent systems" encompass a wide range of applications, including healthcare technologies and eye-tracking software. In instances of connectivity disruptions,

immediate data transmission may not be feasible. However, functional models must exist to support ongoing research in these areas. These processes should not pose significant challenges and must be capable of seamless integration. As technology continues to advance, the functionality of these applications increasingly depends on the widespread use of memristors.

Memristor Neural Networks

Memristor models have numerous applications in the field of computer science. One notable example is their use in the construction of neural networks capable of retaining information. By assigning weight values to connections, memristor models facilitate efficient data processing with minimal power consumption. These models are designed to function similarly to the brain in computing systems. Such neural networks are sometimes referred to as "memristive neural networks." Although the fabrication of real memristors remains challenging and costly, there is no need to rely on actual memristors for the development and testing of neural networks. Instead, models of memristors can be employed. These models provide an affordable and practical means for researchers to create and enhance memristor-based neural networks, accelerating progress in the field. Moreover, this technology can be applied to reconfigurable computing systems, which are characterized by their adaptability, enhancing both their performance and versatility. In essence, these systems are well-equipped to leverage emerging computational technologies. Memristors, which can alter their resistance in response to learned data, offer a promising avenue for the development of such systems. Emulators for memristors are available, enabling professionals to experiment with these devices, refine circuits, and optimize their functionality.

Memristors are challenging to develop due to their high cost and the significant amount of time required for their construction. The Knowm memristor, which is already commercially available, represents a notable advancement, though further research and development are still necessary in this field. The initial memristor that became available for purchase was based on bioinspired technologies that function effectively only under specific conditions, as the damage incurred could not be repaired. Currently, there are memristor replicas that closely resemble the original design, which are constructed using a variety of electrical components. This category includes functional transconductance amplifiers (OTAs), current feedback operational amplifiers (CFOAs), second-generation current conveyors (CCIIs), and others. Understanding the operation of these circuits is complex, as they often incorporate MOS power transistors, operational amplifiers, and electrical multipliers.

2.3. Memristor for Applications in Neuromorphic and Edge Computing

The memristor model circuit is one of the most important components in this context. It is shaped like the end of a curve and has the ability to change its resistance when an external power source is applied. The term "memristor" is particularly apt because its behavior closely resembles that of a memory resistor. Memristors, along with low-power devices, enhance efficiency in various applications. They are particularly valuable because they retain data even when power is lost. Engineers and scientists are increasingly exploring memristors, recognizing their potential for power conservation. They are durable, have a long lifespan, and operate at higher speeds.

Although memristors are highly beneficial, they were not realized until 1971, when Leon Chua published a seminal work. In his study, Chua introduced the concept of this nonlinear

component, positioning it alongside linear resistors, capacitors, and inductors in electrical systems. This fourth basic two-terminal device, however, differs significantly from RLC networks. While memristors were initially a theoretical concept, their practical implementation became a reality when Stan Williams and his team at HP Labs successfully developed the first functional memristor. This breakthrough demonstrated the viability of memory resistance as a fundamental property of small-scale systems. When an external voltage is applied, the current and voltage within the memristor fluctuate considerably. Upon applying a bias voltage, the memristor can change states and retain the last state, a process facilitated by an I-V pinched hysteresis loop. As a result, the memristor is likely to be the fourth critical element in electronic systems. CMOS microcontrollers have since examined memristors due to their ability to retain data even when changing states, offering significant advantages in terms of data persistence and power efficiency.

Memristors are not solely utilized for data storage in most cases. They are not primarily used for DRAM due to their comparable speed and thickness. A variety of advanced applications also leverage them. For example, memristors can model synaptic neurons, an essential step toward developing computers that mimic brain cells. Bio-systems that function similarly to computers are used by brain-like computers to store and process data, achieving a more efficient performance. These systems help maintain cognitive calmness, which is beneficial for complex tasks. A recent study presents a new form of memristor-like device, which consists of nine transistors and a single closed capacitor. This circuit can be transformed into an integrated circuit (IC) even if some components fail. The paper discusses modifications made to CMOS-based memristor model circuits, enhancing their suitability for low-power edge computing. This improvement is facilitated by the MOS capacitance within the memristor. For individuals familiar with 45 nm and 16 nm CMOS technology, replicating the design presented in the paper is feasible. The memristor in question incorporates four pMOS transistors, five nMOS transistors, and a grounded capacitor. The remainder of the study paper is structured as follows: Given the understanding of their function, constructing such a memristor is straightforward. The paper outlines the mathematical models and research conducted on the specified memristor. It also provides an overview of the practical implementation and the discussions held regarding future developments in this area.

3. Method

The DVS camera is capable of detecting movement in the nervous system, resembling the way the brain functions in certain aspects. It can quickly identify and learn rapid movements due to its brain-like operation. Additionally, it is energy-efficient, handling high levels of light while consuming minimal power [28]. This efficiency facilitates the processing of live video, enabling real-time tracking of movement. The events captured by the DVS camera are illustrated in Figure 1a of the dataset, which provides detailed information regarding the occurrence of each event, including the time, x-coordinate, y-coordinate, and direction. By analyzing the x- and y-coordinates, the location of each event can be determined. The direction indicates the relative brightness or dimness of the light. An example of how events accumulate over time is depicted in Figure 1a. Within the specified time frame, the number "0" could have been recorded as many as 30,000 times. The DVS camera operates with a resolution of 128 x 128 pixels, and it is evident that faster movements result in more events occurring within a

given period. Consequently, the DVS camera is more sensitive to rapid motion than to slower movement. Figure 1b illustrates the progression of the POKER-DVS dataset over time, with a line graph demonstrating the accumulation of events within the stream, which totals approximately 4,000 events over the years.

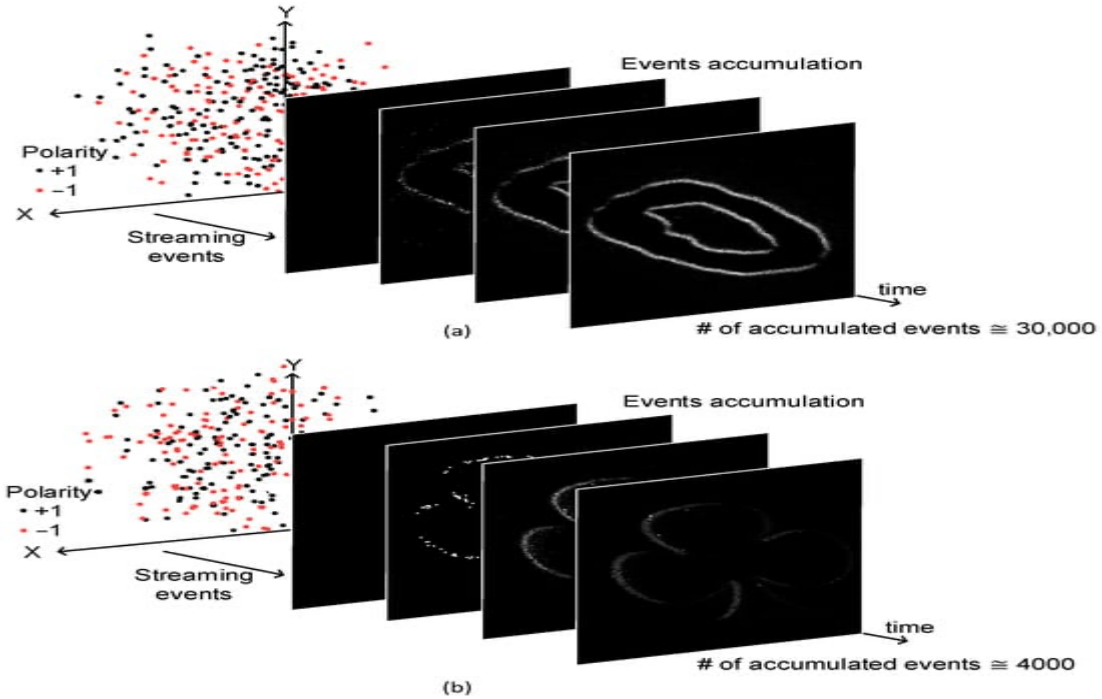

Figure 1. (a) The MNIST-DVS dataset's streaming events accumulated over time; (b) the POKER-DVS dataset's streaming events accumulated over time.

A block model of a memristor–CMOS smart circuit is presented in Figure 2a. These components are employed to observe the live events captured by the DVS camera. The events being streamed are depicted on the left side of Figure 3a. On the right side of Figure 2a, the event-driven neural networks utilized in this study are shown. These networks consist of CMOS and memristor components. A synaptic memristor bridge is positioned at the center of the hybrid circuits. The rows and columns of the crossbar are connected to neurons that store information related to both input and output. At the bottom, a master device controls the timing of MAC calculations and powers itself off to conserve energy.

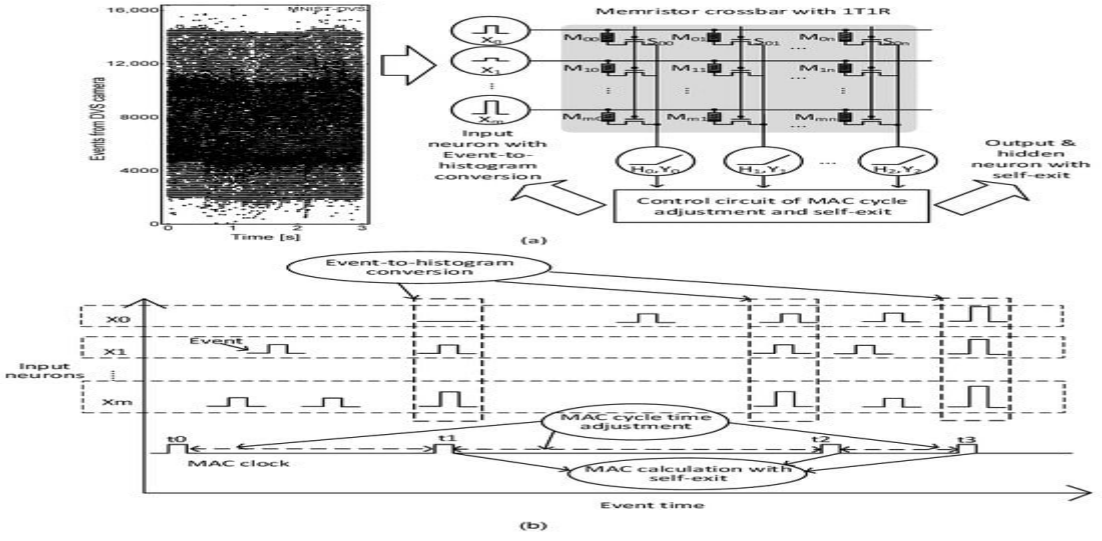

Figure 2. (a) Memristor–CMOS hybrid circuit timing diagram explaining self-exit and MAC clock modification; (b) Memristor–CMOS hybrid circuit block design for DVS camera event processing.

The following steps must be taken to complete the process. The DVS camera, depicted in Figure 2a, records events intermittently. These events, occurring at various times within the stream, are represented by black dots. The events captured by the DVS camera are subsequently used to construct the histogram shown in Figure 2a. The individual events, which take place at different times, are then transmitted to the neurons responsible for processing them. What do X0, X1, and Xm represent? These denote the states of the newly introduced neurons. In this context, "m" represents the total number of newly added neurons. Votes are employed to illustrate how the graph data has been altered in the incoming neurons. The frame of the neural memristor, as depicted in Figure 2a, is shown connected to these neurons. What are the memristor cells within the frame? Ohm's law can be utilized by the brain to determine the amount of current passing through each cell. The column current of the crossbar can be calculated by summing the currents passing through all the memristor cells within the column.

The number can be sent to the secret or output neurons, as it corresponds to the column's MAC formula. The letters Y0, Y1, and Yn can be used to determine how the secret or output neurons are activated. The number "n" indicates the total number of secret and output neurons. Figure 2a illustrates how the control circuit can process the activations of the output and secret neurons, based on their respective activation functions. In order for the controller to make a decision based on the events received, it may send the self-exit signal to terminate the processing clock for the MAC. This is an efficient method of halting the MAC's operation, preventing unnecessary handling of multiple input events when not required. Additionally, it is important to note that the control circuit can adjust the frequency at which the MAC makes decisions, depending on the volume of simultaneous events. When the DVS camera records numerous events, the MAC takes longer to process. Conversely, if events occur infrequently, less processing is needed, and the MAC clock will slow down. The time diagram for a hybrid memristor–CMOS circuit is presented in Figure 3b. These components observe the data from the DVS camera to understand the ongoing events. The incoming neurons are depicted along the y-axis, labeled X1, X2, and Xm. The sensitive neurons are informed of every action recorded by the DVS camera. It takes progressively longer for the events in the first row of Figure 3b to reach the input neuron, X0. The second row of events is centered around brain cell X1. At times t1 and t3, the driver initiates a clock on the lower section, as shown in Figure 2b. Upon triggering the MAC clock at time t1, the hybrid circuits take responsibility for the MAC calculations based on the event data from the specified time period. The MAC value at time t2 is determined from the event plot data.

The data presented on the graph from time t0 to time t3 are also utilized to calculate the MAC at time t3. The MAC clock can be deactivated by setting the self-exit flag. Subsequently, the clock can be adjusted based on the number of events processed, thereby reducing power consumption associated with undesirable activities. Additionally, Figure 3a illustrates a circuit comprising input neurons that can transition from an event-driven mode to a histogram-based mode. The resistor Rref and the memristor Rm are depicted in Figure 4a. Each switch is labeled SW0, SW1, and SW2, representing events that occur rapidly over time. By placing a resistor between Rm and Rref, voltage V1 is observed. V1 is then input into the voltage memory of

operational amplifier OP1. Once the voltage reaches its peak, it becomes V2. Figure 3a also includes a pulse generator (PG), which is driven by the MAC clock signal. The role of the pulse generator is clarified in Figure 4b, where it is shown that PG controls X0, a synaptic crossbar.

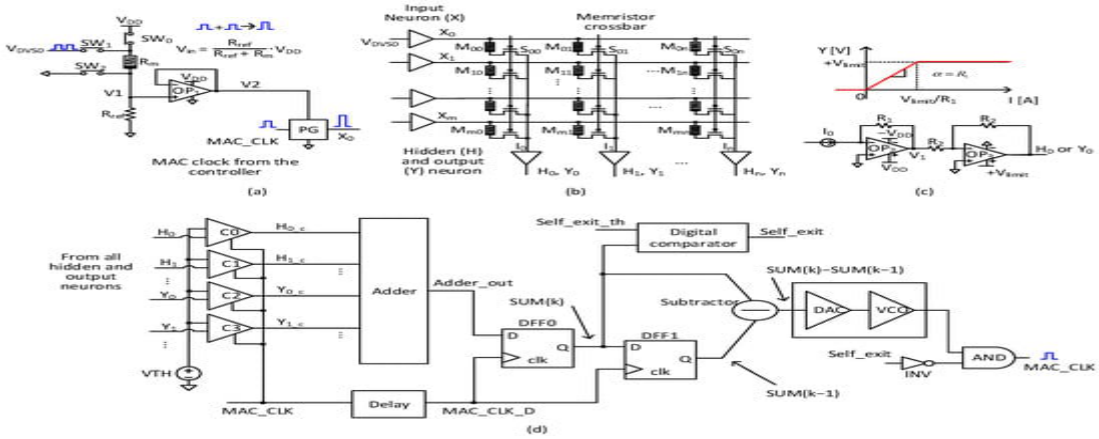

Figure 3. A circuit for adjusting the MAC frequency and self-exit; a synaptic memristor crossbar; a hidden/output neuron circuit with a ReLU activation function; an input neuron circuit with an event-to-histogram conversion (a); and more.

Here is a description of how Figure 3a operates. When the input signal is low, SW0 is open to the external environment, while SW1 and SW2 remain closed. During this state, events can be allowed to reach the input neuron. As more events occur, the conductance of Rm gradually increases to compensate. When the input signal is high, SW1 and SW2 are open, and SW0 is closed. The time it takes for the MAC (Multiply-Accumulate unit) to determine when the input signal is high is determined by Rm, which represents the constant. If 'MAC_CLK' is low, the conductance of Rm changes slowly, and V1 may increase. X0 indicates that V1 can influence the output more by providing additional information to PG based on its observations up to that point. By tracking the number of spikes sent by the DVS camera, the strength of X0 can be used to display the data in a graphical format, as shown in Figure 4b. The sets of bars in Figure 3a are associated with X0, X1, and Xm. These values change as the signals from the nerve cells are received. M00 and S00 function as 1T-1M cells in this context. I0, I1, and In represent the column currents in the crossbar array.

In Figure 4b, the word is displayed on the output neurons, corresponding to the values represented by Y0, Y1, and Yn. For instance, the characters H0, H1, and Hn represent the outputs of the three hidden neurons. The columns of the memristor bars are connected to both the hidden neurons and the output neurons, as depicted in Figure 4b. Figure 3c illustrates a circuit example featuring both an output neuron and a hidden neuron using a ReLU. I0 refers to the location where the crossbar intersects. It is understood that H0 or Y0 represents the voltage of a hidden or output neuron, and I0 corresponds to its column current, as shown in Figure 4c. This device converts electrical current into voltage. The two components are denoted as OP2 and OP3. R1 and R2 are distinct from one another. It is critical to note that Vlimit must be employed to prevent further voltage variation, as depicted in Figure 4c. The activation function in Figure 4c closely resembles the ReLU function, which is commonly utilized in advanced computing systems. A control unit, as shown in Figure 3d, can adjust the MAC frequency and then maintain it. In this case, the values H0, H1, Y0, and Y1 are derived from

the hidden neurons and output neurons in Figure 4c.

The variables C0, C1, C2, and C3 can be utilized to construct analog comparators. When the threshold voltage (VTH) is established as the reference voltage, this check verifies whether H0, H1, Y0, and Y1 are all equivalent. It is crucial to note that the comparators will only function if the signal is high. They deactivate when the signal is low, ensuring no power consumption. These comparators are denoted as H0_C, H1_C, Y0_C, and Y1_C, representing the states communicated by the system. These ports transmit binary values, either 0 or 1. If H0 exceeds VTH, H0_C will output 1; otherwise, H0_C will output 0. As illustrated in Figure 4d, the digital data resulting from the comparison is forwarded to the adder. In Figure 4d, the output represents the adder's operation, specifically indicating the number of hidden and output neurons activated at levels exceeding VTH. The sample DFF0, as shown in Figure 3d, is transmitted, which is related to a signal integral to the package. The 'Adder_out' is captured by 'MAC_CLK_D' when 'MAC_CLK' is high (as seen in Figure 4d). After identifying the MAC, this step is executed.

The output from DFF0 is connected to the output of DFF1. When configured in this manner, both DFF0 and DFF1 can store "SUM(k)" simultaneously. The current value of "Adder_out" is compared to its previous value. The difference between \(k\) and \(k - 1\) can be converted into an analog signal using a Digital-to-Analog Converter (DAC). The DAC's output voltage may be significant if the difference is large. This voltage powers a Voltage-Controlled Oscillator (VCO), which increases its frequency in response to higher DAC output voltages. Conversely, when the DAC's output voltage is low, the VCO reduces its frequency. In Figure 3d, a signal is generated when "SUM(k)" exceeds a specified base value, which determines the number of active hidden or output neurons. If the number of active neurons exceeds this preset value, a "Self_exit" flag is sent to the CPU, as depicted in Figure 3d. An "INV-type" inverter initially receives the "Self_exit" signal. The output from this inverter is then sent to an "AND" gate. For the "MAC_CLK" to function, the "Self_exit" signal must be high. When "MAC_CLK" is disabled, the memristor-CMOS hybrid circuits shown in Figure 3 may not consume additional power.

Patterns are used in Figure 5 to illustrate the signals that control the variation in MAC frequency and self-exit. Figure 3d provides a depiction of what these signals represent. In Figure 4d, the signal "MAC_CLK" is shown, which activates the C0, C1, C2, and C3 components of the analog comparator. Both the "H0_C" signal and others can be observed coming from the comparator. This signal can be detected when "MAC_CLK" is high. In Figure 5, the values that have been calculated are stored in DFF0 and DFF1, where the numbers are input into the adder. This set of values is near the start of "MAC_CLK_D." Thus, "MAC_CLK_D" represents the delayed version of the "MAC_CLK" signal. As previously mentioned, the terms SUM(k) and SUM(k - 1) in Figure 4 indicate the current and previous values, respectively. When the DVS camera operates at a high speed, distinguishing between k and k-1 is crucial. However, this distinction becomes irrelevant when the DVS camera operates at a lower speed. As seen in Figure 4, altering the gap between k and k-1 changes the "MAC_CLK" frequency. For the signal to become sufficiently strong, a specific number of

active hidden and output neurons is required. It is evident from Figure 4 that the "MAC_CLK" signal ceases when the "Self-exit" value exceeds a certain threshold.

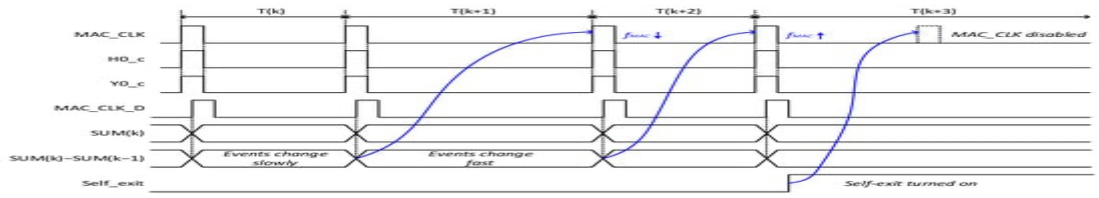

Figure 4. The signal waveforms in the MAC frequency adjustment and self-exit control circuit.

The digital section of the neural network driver is depicted in Figure 4d, while Figure 5 illustrates the associated details. A key factor contributing to this design is the Generic PDK based on 0.18 µm CMOS technology, which is available with CADENCE software. This technology was utilized to develop the circuits shown in Figure 5. The circuits presented in Figure 6 were designed in accordance with CMOS design standards, allowing for scalability. With smaller CMOS technologies, such as 0.13 µm, these circuits can be easily adapted with minimal effort by the designer. The DAC and VCO are presented in Figure 5, and they can be reproduced due to their implementation in Verilog-A, a computer language that effectively models the behavior of the circuits. The operational models of the DAC and VCO were developed using empirical data derived from the fabricated chips.

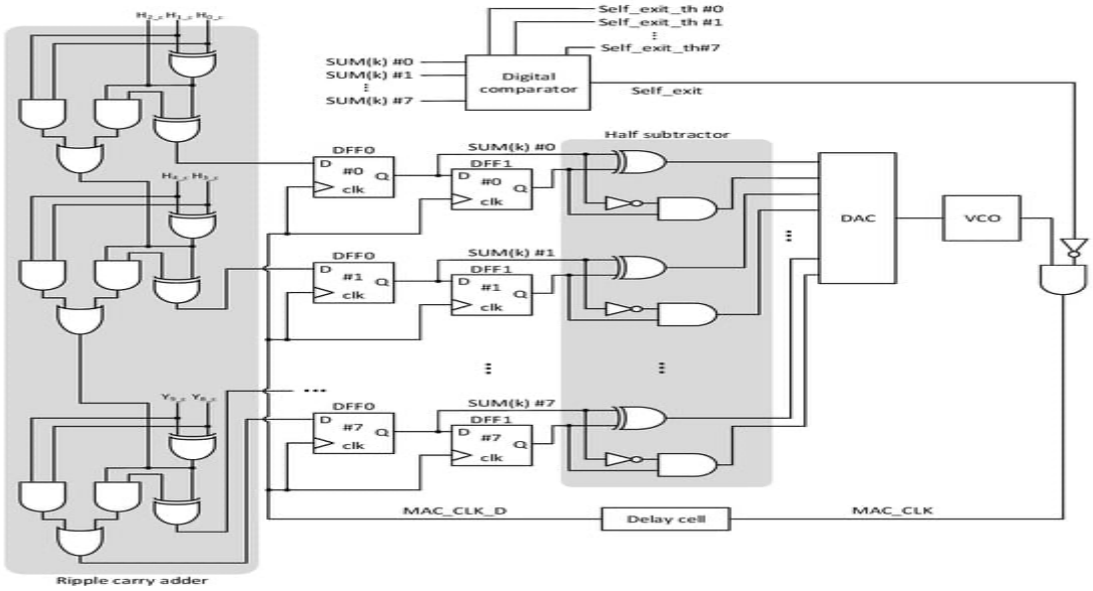

Figure 5. The controller circuit architecture of the neural network for MAC frequency change and self-exit.

4. Results and Analysis

Figure 6 provides a clear representation of the composition of a memristor. For \(w = 2w_0 \), the sine function incorporates a harmonic with a voltage (\(V \)) of 1 V and a frequency of 1 Hz (\(V(t) = V_0 \sin(wt) \)). Since \(V \) is a negative voltage, the current (\(I \)) increases when a negative charge is applied, and decreases when a positive charge is applied. This behavior improves the overall system. Additionally, it is evident that the flow of current and the charge are directly related in a linear manner.

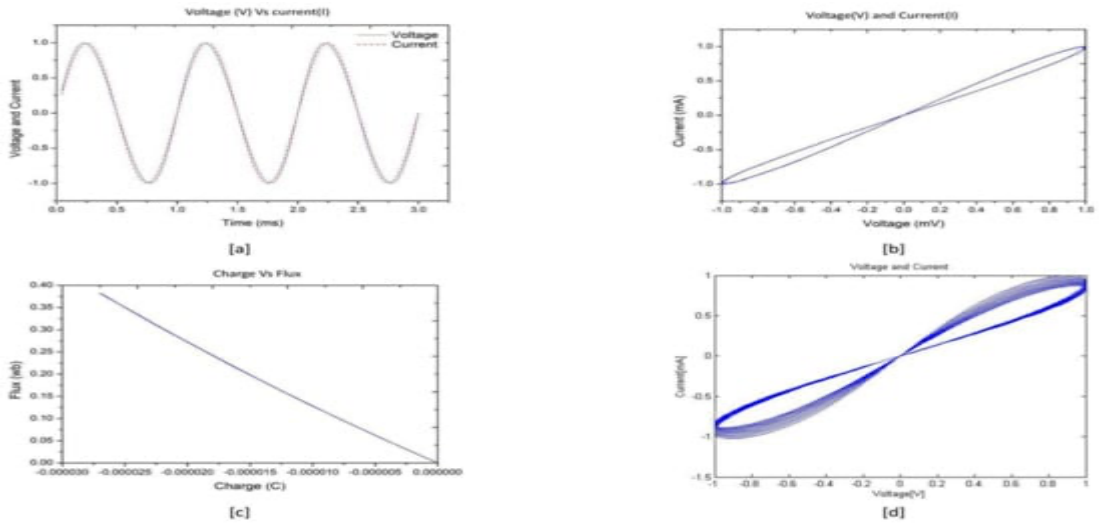

Figure 6. The basic memristor's MATLAB simulation results. (a) sinewave input signal; (b) memristor V-ĩ characteristics; and (c) linear charge-flush relationship (d) non-linear properties of a pinched hysteresis loop.

Please see Figure 7. When the incoming voltage is high, the resistance values decrease. Conversely, when the voltage is low, the resistance values increase. This behavior is similar to that of a memristor. When the input signal is strong, more electrical current flows. The process was repeated multiple times, and the results are shown below. The system operates with a high voltage of 0.4 V and a low voltage of ±0.95 V. By connecting Vth to the DC source, the voltage between the gate and the source can be adjusted. The system is configured to connect both the source and the sink in this manner.

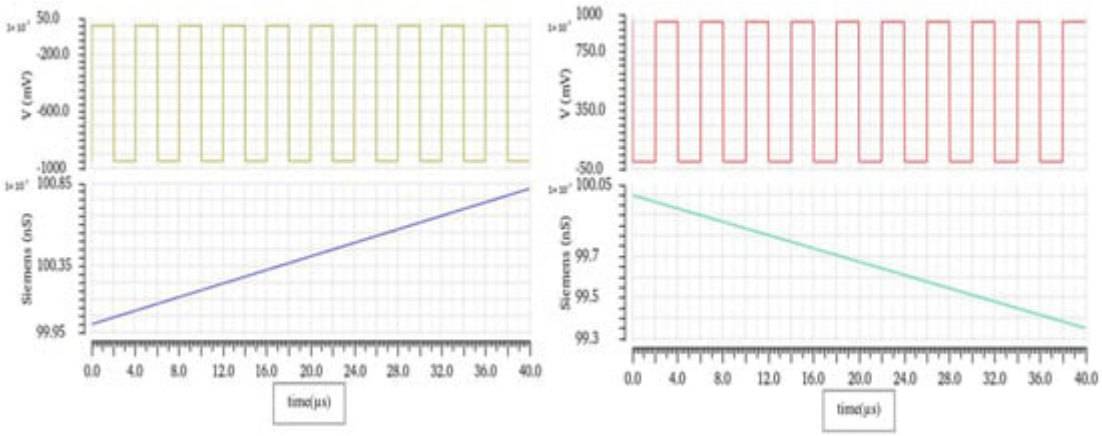

Figure 7. One set of graphs shows the pulse response positively, while the other shows the pulse response in a negative one.

Figure 8 below illustrates the events that occurred in the scenario with the most favorable numbers derived from the IFG model.

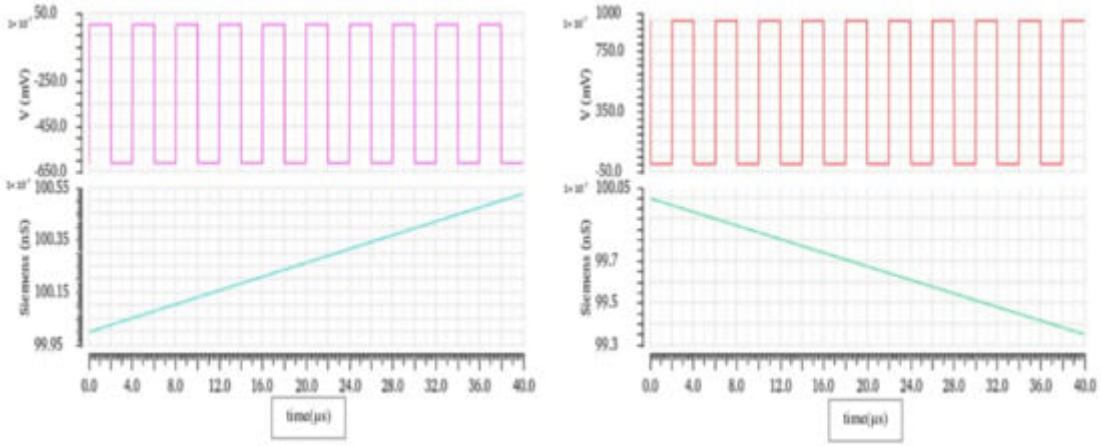

Figure 8. Outcomes of post-simulation for optimal parameters.

Subsequently, the updated values are input into the IFG machine. The following step mirrors the previous one, though it exhibits a 0.8% higher degree of accuracy. From this point forward, the settings should remain stable. Table 1 presents basic memristor values and illustrates how the current varies as the voltage increases or decreases. Tables 2 and 3 display the IFG values derived from simulations using Cadence Virtuoso. The conductance varies with voltage, as indicated by the provided dataset. This article also discusses charge (q), current (I), voltage (V), and flux (Φ), all of which are key factors in memristor behavior. The IFG model demonstrates that the conductance values (Gmax) are correlated with voltage and the Siemens unit.

Table 1. Parametric values for the hysteresis curve in terms of current, voltage, flux, and charge.

# of Measurement	Voltage Coming In (V)	Current coming in (I)	Change (§)	Charge (q)
1.	18 mV	22 mA	3.3 x 10−9 (Wb)	–2.8 x 10−9 C
2.	37 mV	44 mA	1.3 x 10−4 (Wb)	-1.11 x 10−8 C
3.	56 mV	66 mA	1.5 x 10−4 (Wb)	-2.50 x 10−8 C
4.	75 mV	88 mA	1.8 x 10−4 (Wb)	–4.5 x 10−8 C

Table 2. When the input pulse response equals (+0.95 V), parametric value analysis is performed.

# of Measurement	Voltage Coming In (V)	Siemens (ns)	
		Gmax = 107 times 1 (X)	Gmax = 107 times 1 (Y)
1.	95 V	0	1.0×10^{-7}
2.	60 V	2.0×10^{-8}	1.0×10^{-7}
3.	31 V	3.0×10^{-7}	1.0×10^{-7}
4.	19 V	4.02×10^{-6}	8.8×10^{-8}
5.	0	6.02×10^{-6}	8.98×10^{-8}

Table 3. Analysis of parametric values when the input pulse response equals (-0.95 V).

Measurement number	Voltage Coming In (V)	Siemens (ns)	
		Gmax = 1.007(X)	Gmax=1.007(Y)
1.	0	0	1.0×10^{-7}
2.	19 V	2.0×10^{-8}	1.0×10^{-7}
3.	31 V	3.0×10^{-7}	1.0×10^{-7}
4.	60 V	4.0×10^{-6}	1.0×10^{-7}
5.	95 V	6.0×10^{-6}	1.0×10^{-7}

In Table 4, the normal model and the proposed model are presented side by side for comparison. The sigmoid function is utilized in the normal model, while the proposed model employs both the ReLU and Adam activation functions. The recognition accuracy increases by up to 94.6% when these functions are applied to transformed data. This indicates that the proposed approach performs more effectively when implemented.

Table 4. Analytical and optimal values are contrasted.

Model No.	Function of Activation	The Truth
Model from the past	The sigmoid function	82.7%
The proposed model	The Adams function and the ReLu function	83.5%

5. Conclusions

Handling deep learning models in applications that rely on pattern recognition is essential, as they are utilized in many aspects of daily life. The development of an IFG device, functioning like a circuit with rhythm and memristors, would not have been possible without this understanding. To determine optimal values, the gradient descent model is employed. This demonstrates the capabilities of a pattern-recognizing IFG device, allowing for comparison between prior and modified elements. When the IFG model was applied, the neural network showed a 0.8% improvement in accuracy. As a result, the first network achieved 93.8% accuracy, while the second network reached 94.6%. For enhanced image recognition, neural networks utilizing IFG-based memristor features can be employed, as they expedite the training process.

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